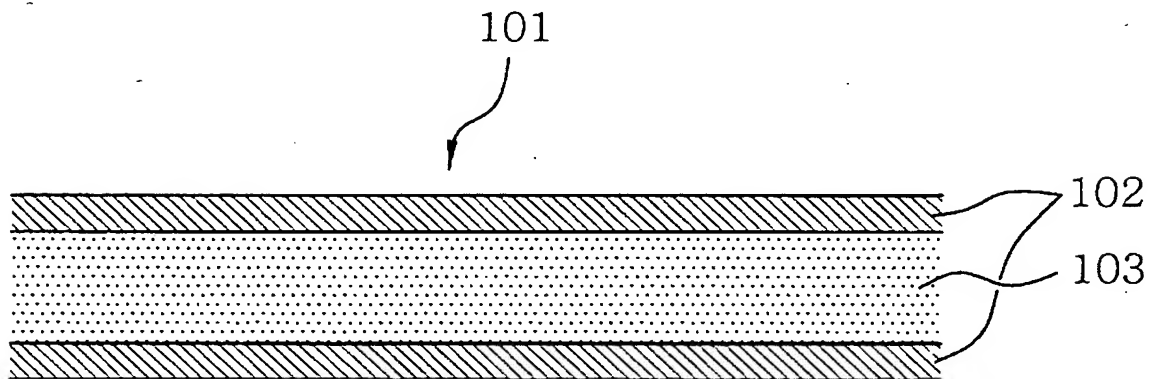


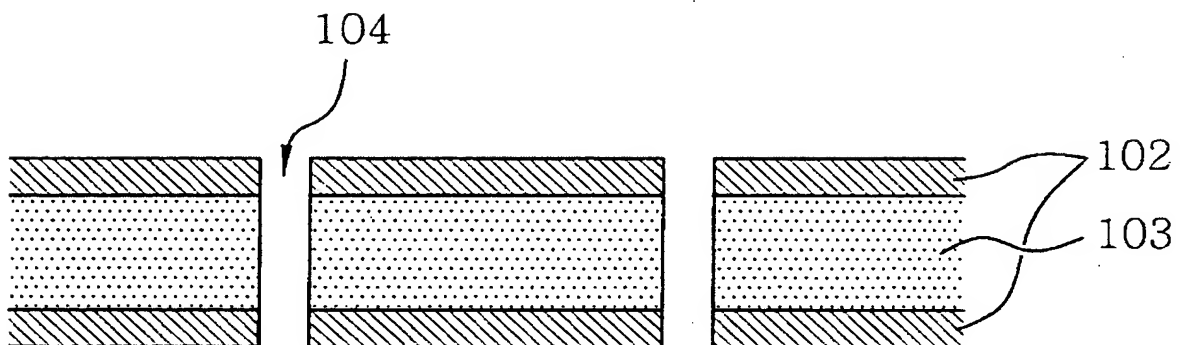
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Fig. 1a
PRIOR ART



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Fig. 1b
PRIOR ART



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Fig. 1c
PRIOR ART

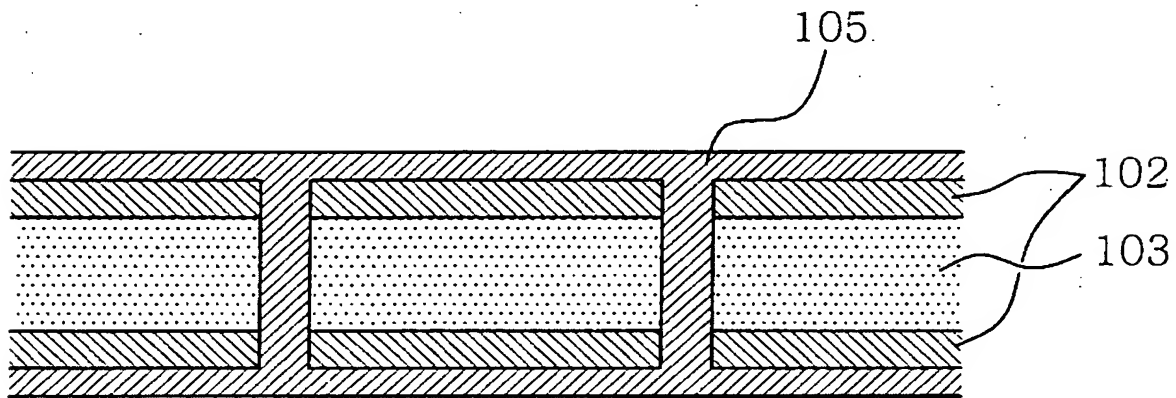
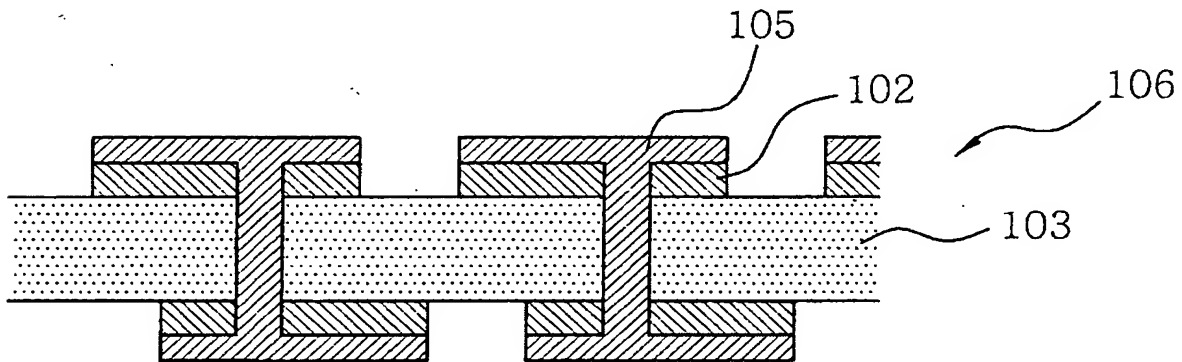


Fig. 1d
PRIOR ART



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Fig. 2a

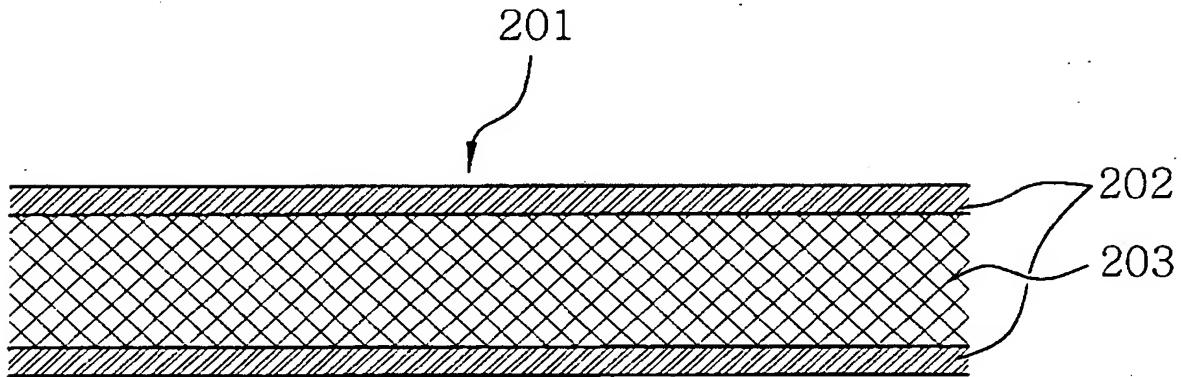


Fig. 2b

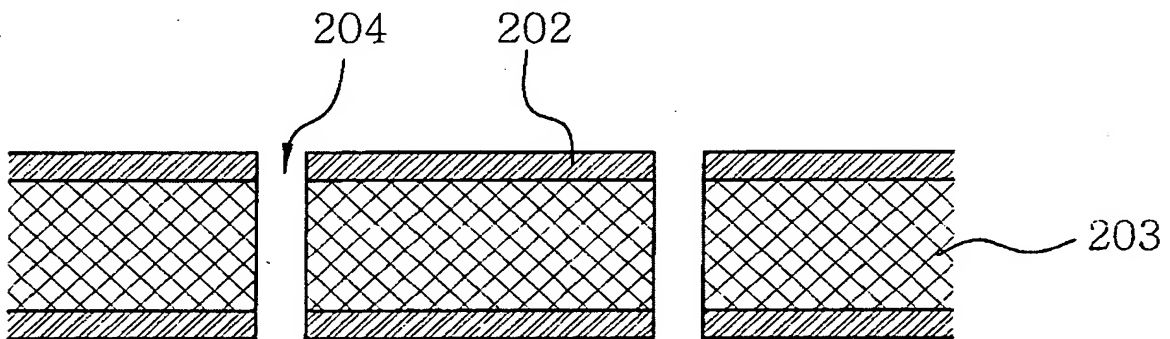
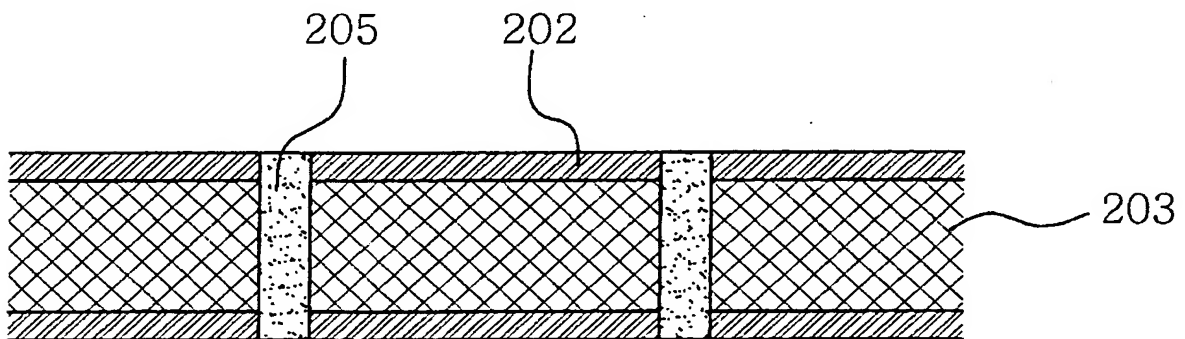
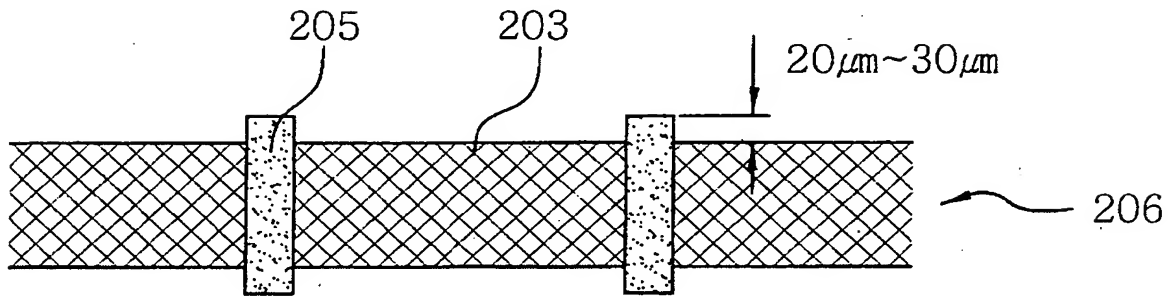


Fig. 2c

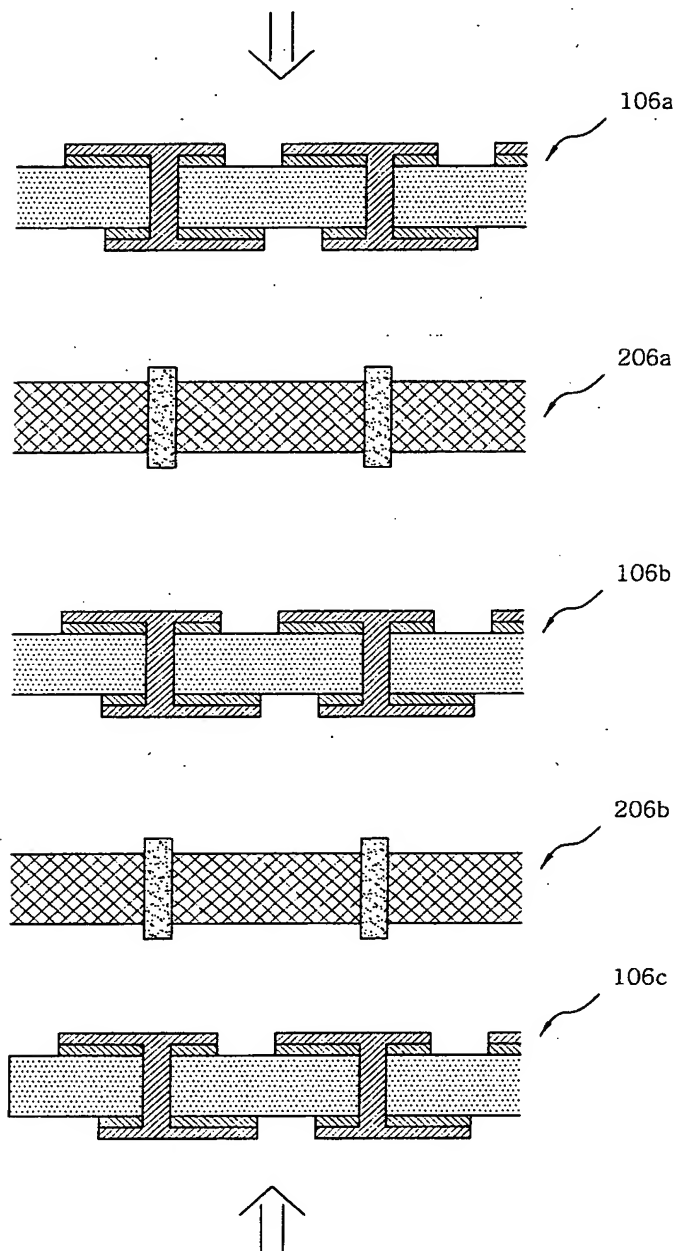


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Fig. 2d



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Fig. 3
PRIOR ART



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Fig. 4
PRIOR ART

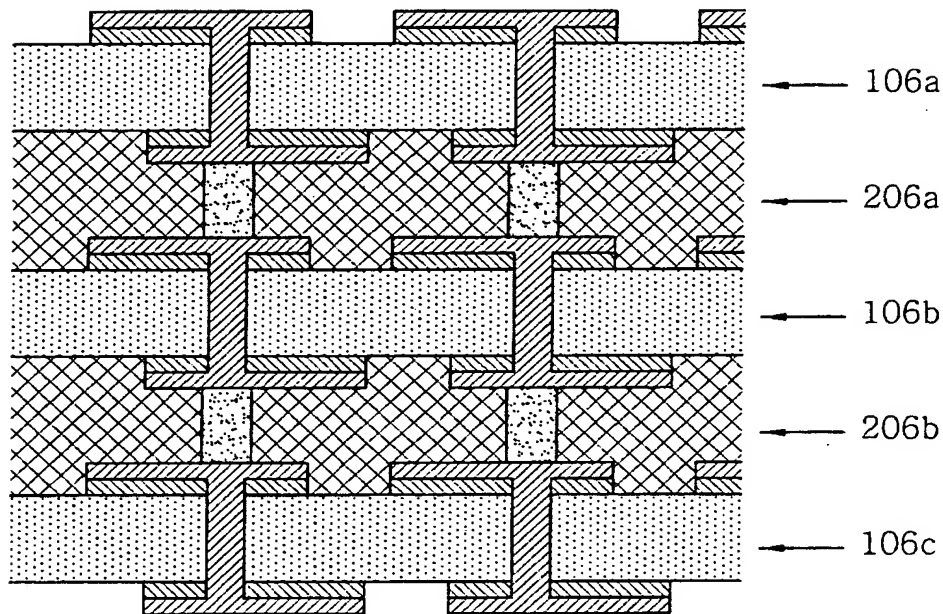
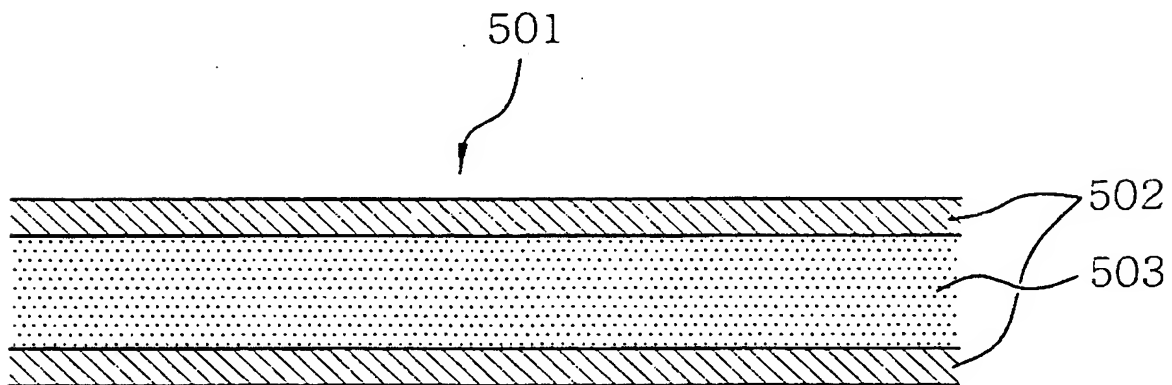


Fig. 5a



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Fig. 5b

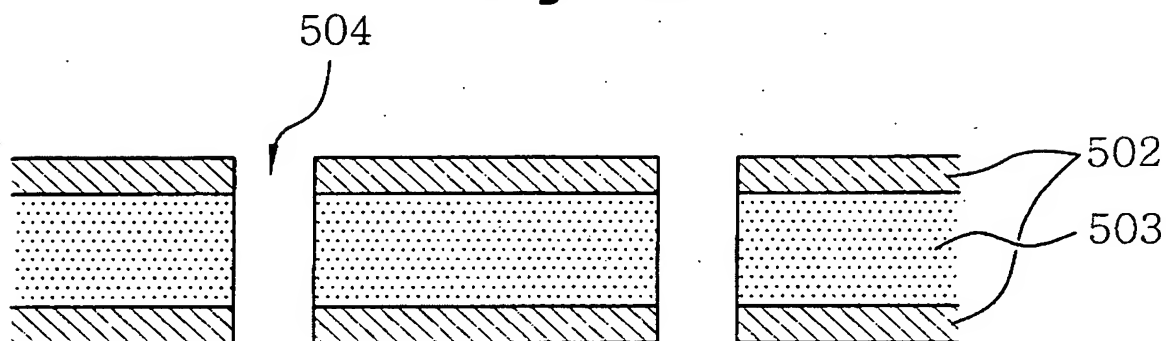


Fig. 5c

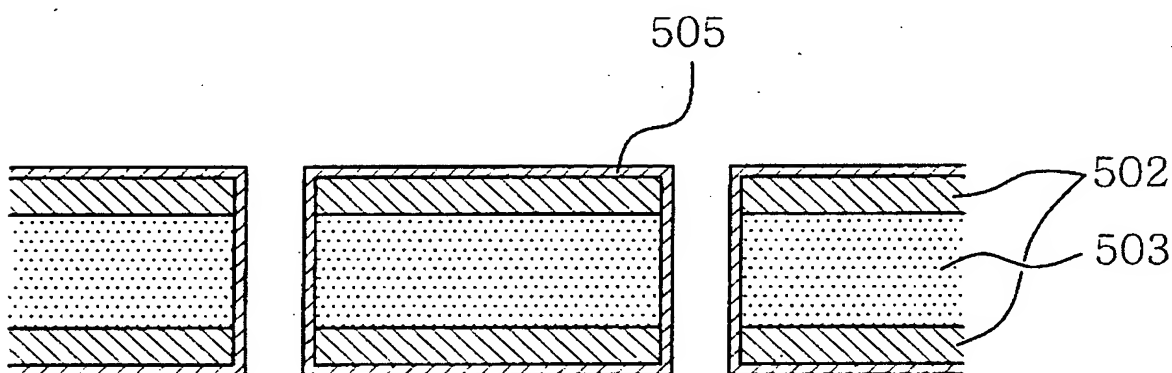
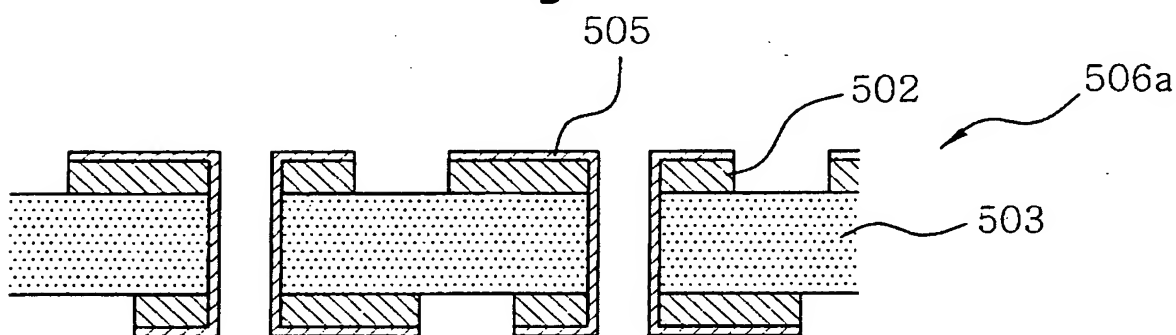


Fig. 5d



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Fig. 5e

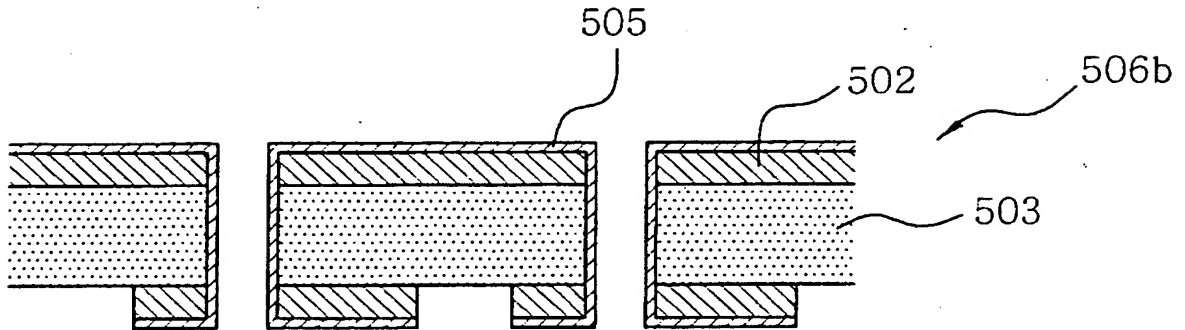


Fig. 5f

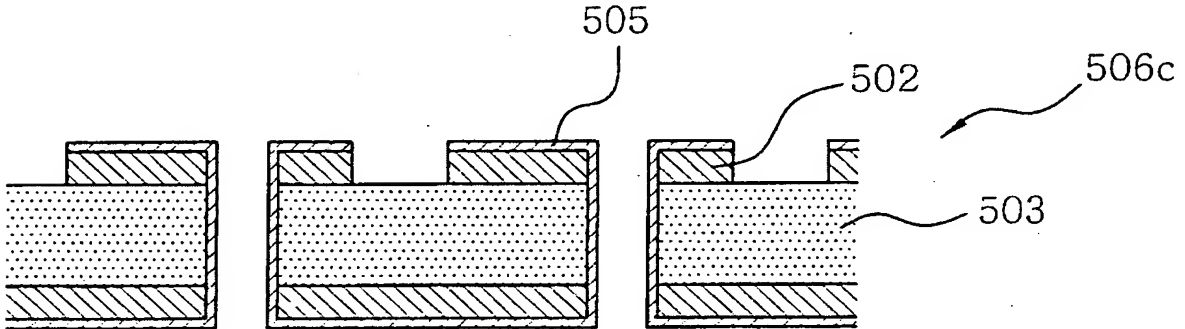
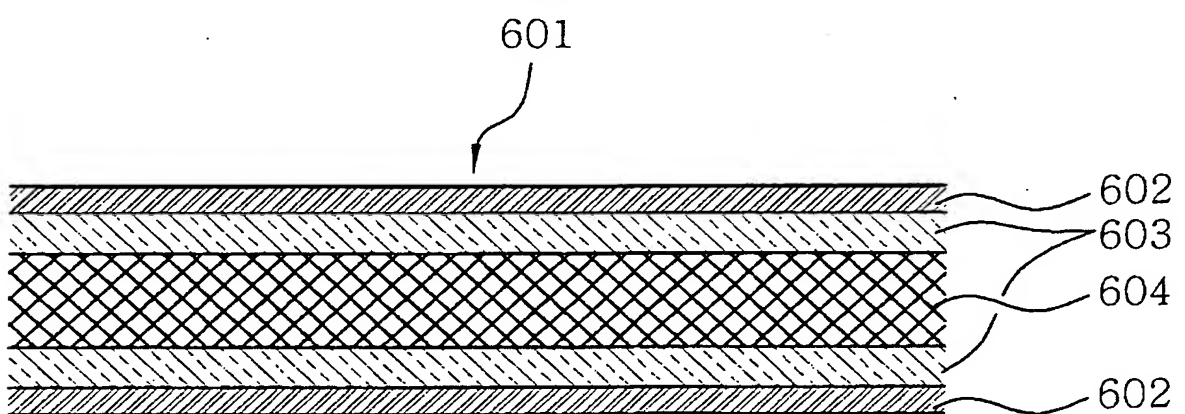


Fig. 6a



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 Fig. 6b

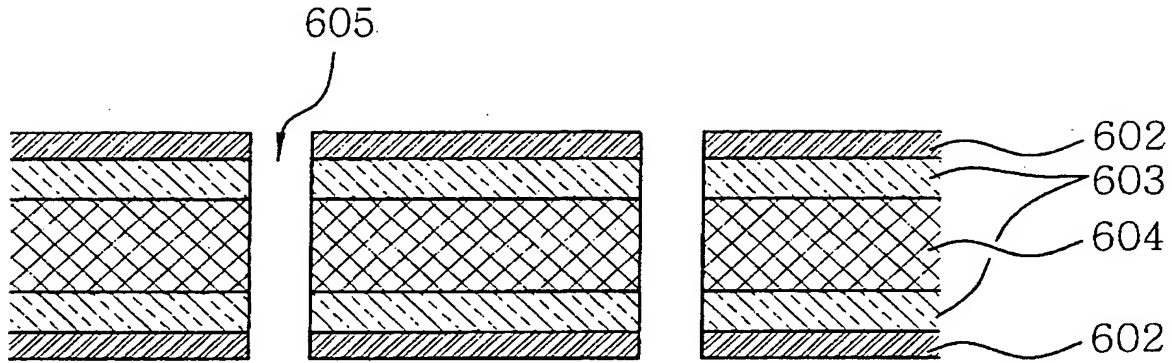


Fig. 6c

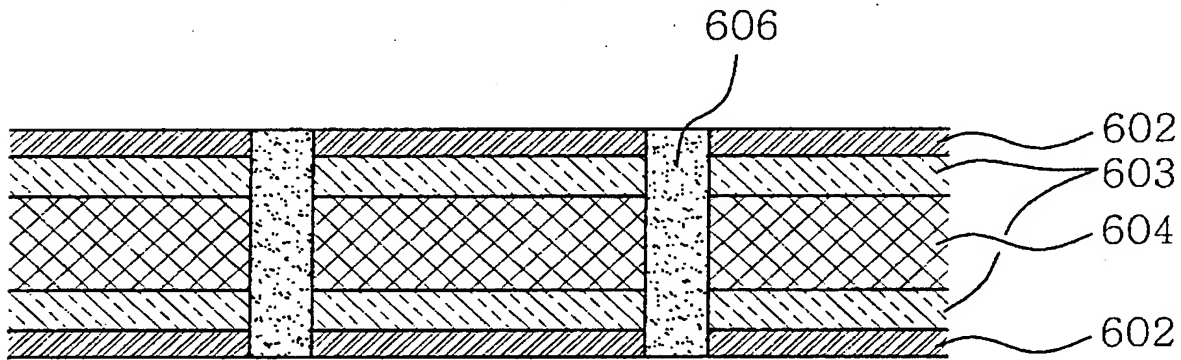
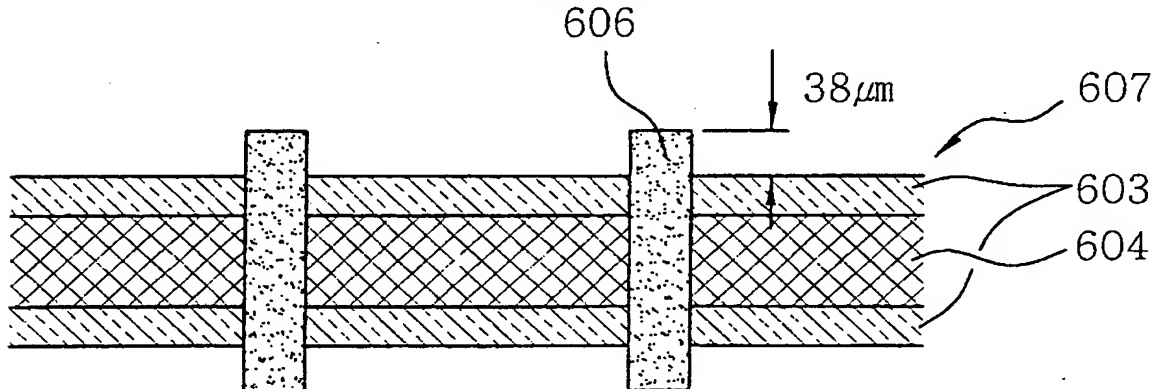


Fig. 6d



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Fig. 7a

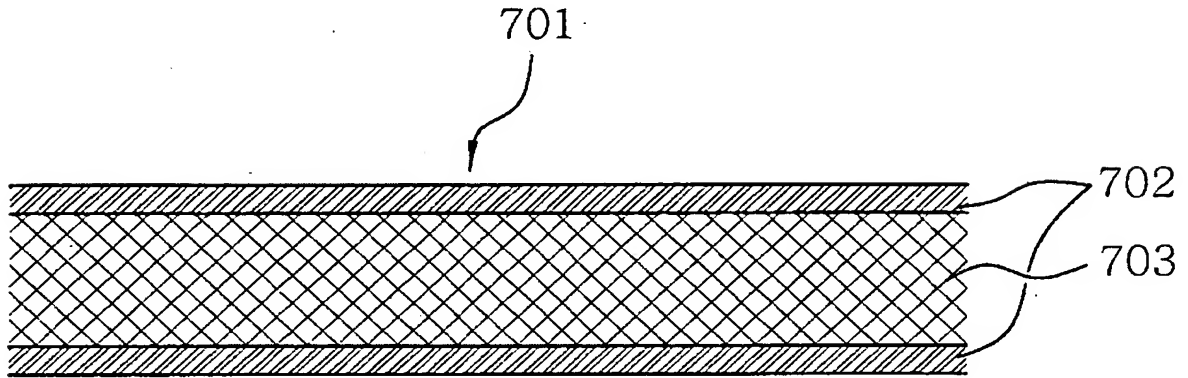


Fig. 7b

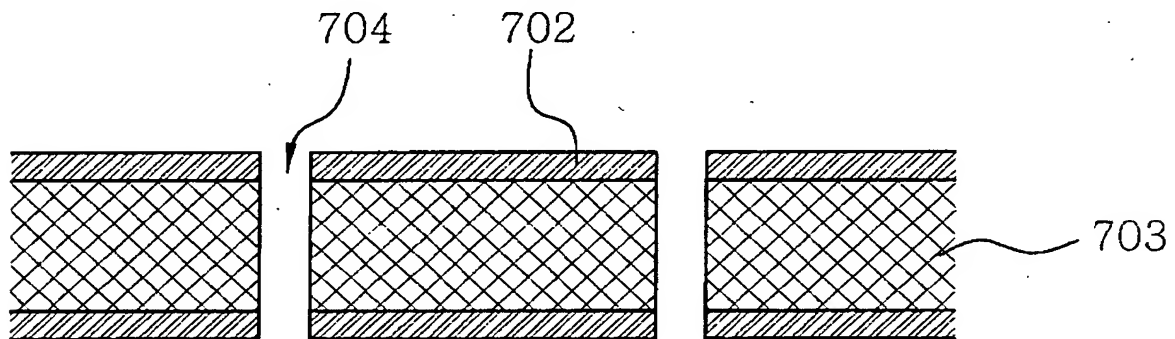
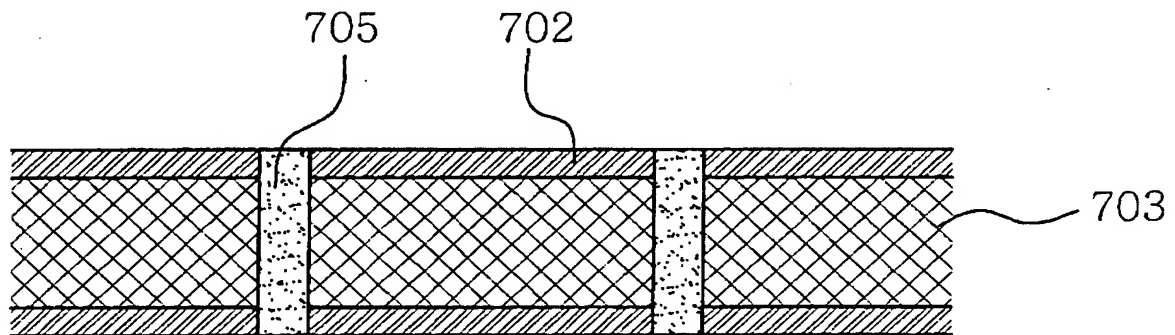
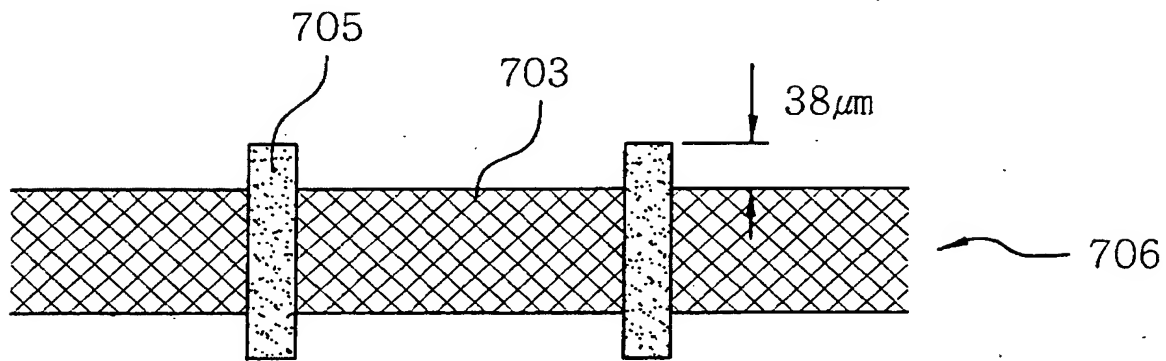


Fig. 7c



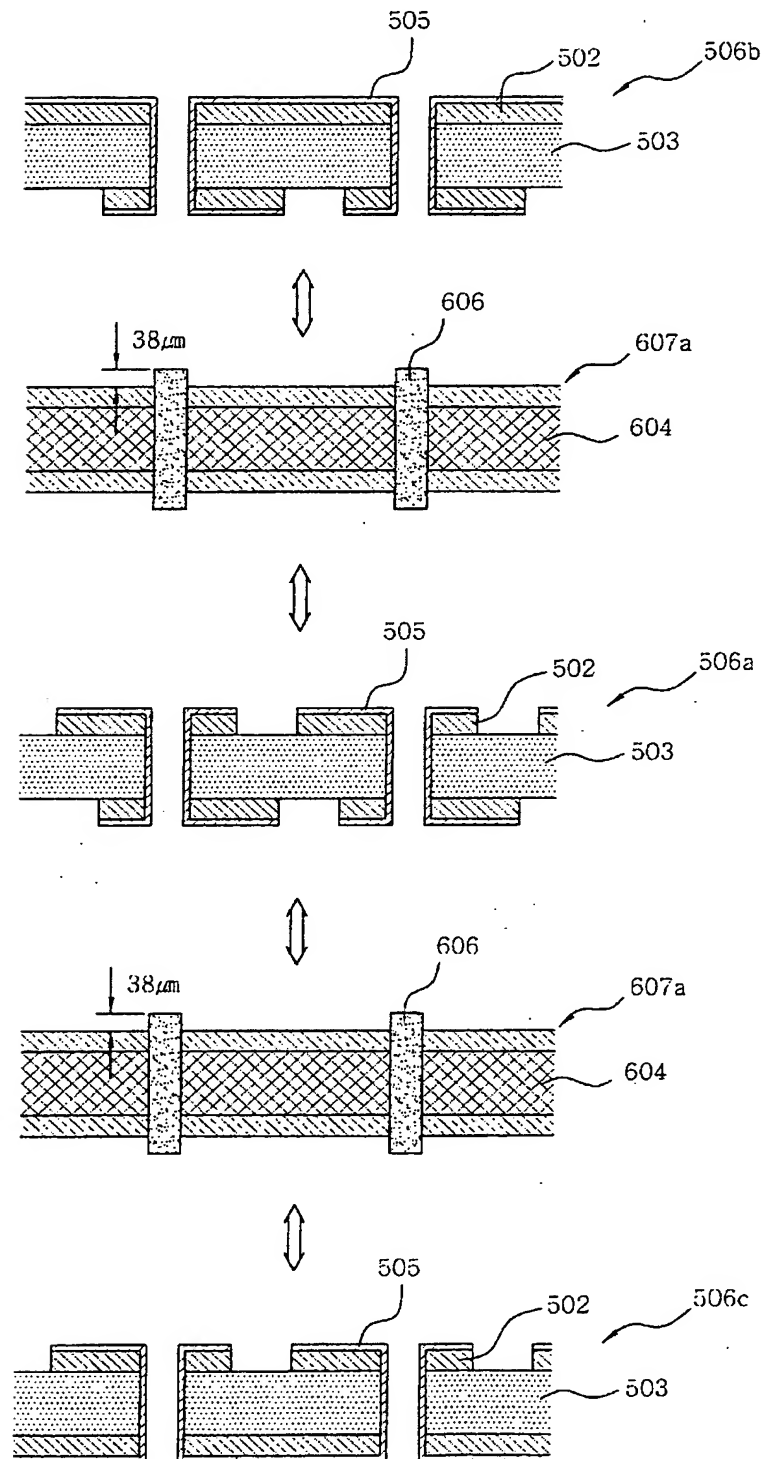
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Fig. 7d



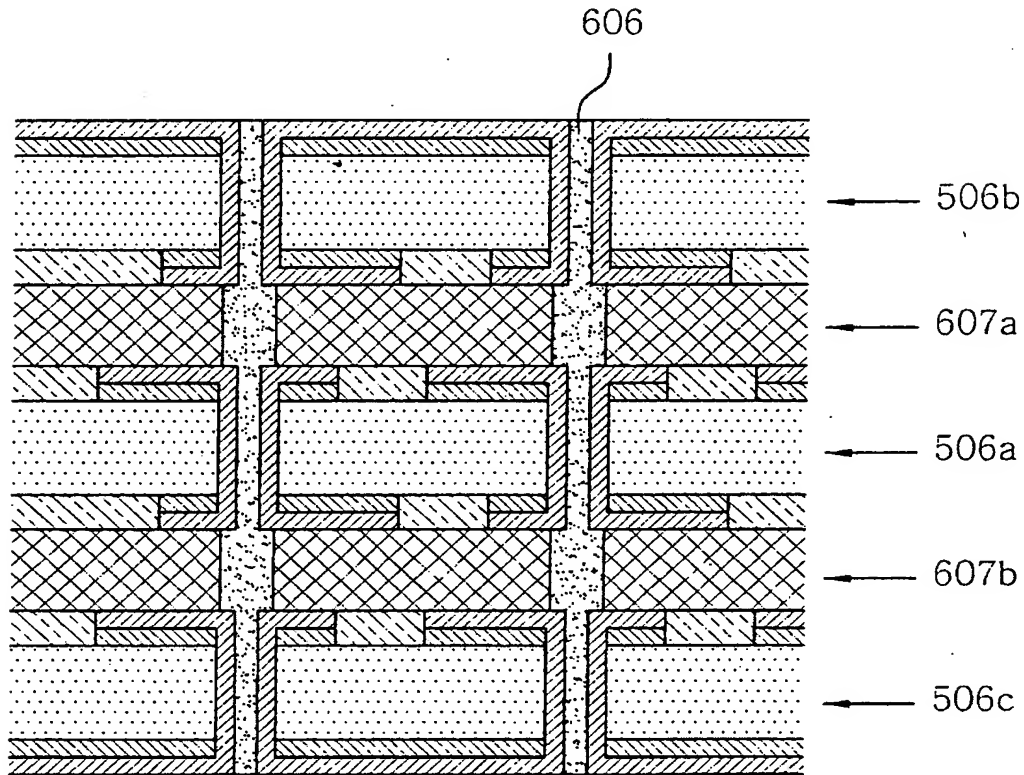
Title: PARALLEL MULTI-LAYER PRINTED CIRCUIT BOARD HAVING IMPROVED INTERCONNECTION AND METHOD FOR MANUFACTURING THE SAME

Inventors: Jee-Soo Mok, Byung-Kook Sun, Chang-Kyu Song, Geum-Hee Yun, Tae-Hoon Kim
Docket No.: LEPA122042

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Fig. 8



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Fig. 9



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Fig. 10

